REMARKS

The following remarks are made in response to the Office Action mailed July 18, 2005. Claims 2-4 and 16 have been cancelled. Claims 1-23 were rejected. With this Response, claims 1, 5, 7, and 15 have been amended. Claims 24 and 25 have been added. Claims 1, 5-15, and 17-25 remain pending in the application and are presented for reconsideration and allowance.

Claim Objections

The Examiner objected to claim 16 because of an apparent missing word. Because Applicant has cancelled claim 16 with this response, however, the objection is not longer relevant.

Claim Rejections under 35 U.S.C. § 102

The Examiner rejected claims 1-5, 7, and 9-23 under 35 U.S.C. § 102(b) as being anticipated by the Wang et al. U.S. Patent No. 5,831,472.

Claim 1 of the present application includes a process variation compensation circuit. The process variation compensation circuit includes a threshold voltage detector circuit, a comparator network, and a compensation circuit. The threshold voltage detector circuit is configured with at least one transistor that is manufactured during a process, and the threshold voltage detector generates an output signal dependant on variations in the process. The comparator network is coupled to the threshold voltage detector and receives the output signal generating responsive logic signals indicative of the output signal.

As amended, the compensation circuit ***includes logic gates*** that are each configured to receive the logic signals, includes a circuit block coupled to the logic gates, and includes at least one transistor manufactured from the process. The circuit block is configured to receive outputs of the logic gates and to adjust the circuit block according to certain outputs of the logic gates. The circuit block is configured as an inverter, and ***the adjustment to the circuit block includes, dependent on the outputs of the logic gates, adding a transistor to or removing a transistor from the inverter***. Support for the amendments for claim 1 are found at least in the specification page 14, lines 20-31, page 16, lines 10-26, dependant claims 13 and 14, as well as in Figures 5

and 6. Since none of the art of record teaches or suggests a compensation circuit with logic gates having outputs that add a transistor or removing a transistor from an inverter, claim 1, as amended, is in condition for allowance over the art of record.

The Wang (US 5,831,472 A) reference discloses an integrated circuit that allows tracking and compensation for shifts in a line receiver's input threshold caused by manufacturing process parameter and temperature variations. As shown in Figure 4, the circuit comprises an input threshold reference circuit 42 which develops a steady-state input threshold. Input threshold references and reference voltages are compared by a comparator network comprising the elements 32-40. Depending on the comparison, the different between the steady-stated input threshold and its design value, additional pull-up or pull-down transistors 58-64 are switched into the conduction leg of a line receiver 48, in order to adjust the line receiver's input threshold to a value within the design input threshold margin budget.

According to the Wang reference, inverters 39 and 41 are arranged between the outputs of the comparators 38 and 40 and the compensation transistors 62 and 64. Inverter 41 is configured to receive a logic signal of comparator 50 and inverter 39 is configured to receive a logic signal from comparator 38. Each inverter 39 and 41 is configured to receive only one of the logic signals and ***not*** both logic signals as it is defined in amended claim 1. The use of the logic gates as described in the present application allows designing compensation circuits which are configured to compensate for manufacturing process effects on either NMOS transistors ***or*** PMOS transistors. Wang discloses compensation circuits which are configured to compensate for manufacturing process effects on both NMOS transistors ***and*** PMOS transistors.

The compensation circuit as defined in new claim 1 can be used in combination with the special detector circuits as shown in Figures 2B and 2C. Conversely, the Wang reference does not teach or suggest a detector circuit such as those of Figures 2B and 2C, and does not teach or suggest a compensation circuit that can be used in combination with such a detector circuit.

Furthermore, claims 5 includes a compensation circuit where the threshold voltage detector comprises a NMOS transistor that is manufactured during the process and where the output signal varies according to a threshold voltage of the NMOS transistor. ***The logic gates include an OR gate and an AND gate***, and a first transistor is added to the inverter or removed

from the inverter dependent on an output of the OR gate and a second transistor is added to the inverter or removed from the inverter dependent on an output of the AND gate. Claim 7 includes a compensation circuit where the threshold voltage detector circuit comprises a PMOS transistor that is manufactured during the process and where the output signal varies according to a threshold voltage of the PMOS transistor. ***The logic gates include a NOR gate and a NAND gate***, and a first transistor is added to the inverter or removed from the inverter dependent on an output of the NOR gate and a second transistor is added to the inverter or removed from the inverter dependent on an output of the NAND gate. Support for the amendments for claims 5 and 7 are found at least in the specification page 16, lines 10-26, page 17, lines 4-13 and page 18, lines 16-31, dependant claims 13 and 14, as well as in Figures 5 and 6.

Wang gives no hint that the logic gates, defined in amended claim 1, could be realized as being an OR gate and a AND gate, as defined in amended claim 5, or a NOR gate and a NAND gated as defined in amended claim 7. Therefore, Wang cannot anticipate a process variation compensation circuit as it is defined in any of these amended claims. Since claims 5-14 depend from allowable claim 1, they are also in condition for allowance.

Claim 15 has also been amended and now includes adjusting a circuit block based on outputs of the logic gates and ***dependent on the outputs of the logic gates, adding a transistor to or removing a transistor from the inverter***. In this way, for the same reason detailed above, claims 15 and claims 17-25 that depend from it are also in condition for allowance.

The Examiner also rejected claims 1 and 5-8 under 35 U.S.C. § 102(b) as being anticipated by the Larsen et al. U.S. Patent No. 6,407,611.

The Larsen (US 6,407,611 B1) reference also fails to teach or suggest the claimed subject matter. The Larsen reference describes a system and a method for providing automatic compensation of IC design parameters that vary as a result of natural process variation. Process compensation is implemented, by comparing known reference voltages with a generated difference voltage. The output of the comparison is latched into digital decoding logic which provides a process compensation current to a functional circuit. As can be seen from Figure 4, the difference voltage is generated between two identical diode-connected MOSFETs, which are biased with currents that are known to be different in value. The different voltage is inversely

proportional to the transconductance of the first of the two connected MOSFETs. According to Larsen, the compensation is not based on a simply threshold voltage as suggested by the present application, but by a difference voltage. Using a simple threshold voltage as it is defined in amended claim 1, provides that there is only one detector circuit instead of two parallel detector circuits as it is proposed by Larsen. Moreover, Larsen does not suggest arranging logic gates between the detector circuit and the comparator network as it is defined in amended claim 1. In particular, Larsen gives no hint to use AND gates, OR gates, NAND gates or NOR gates, as it is defined in new claims 5 and 7. Therefore, Larsen cannot anticipate a process variation compensation circuit or a method for compensation as it is defined in the amended claims.

Therefore, Applicant respectfully requests reconsideration and withdrawal of the 35 U.S.C. § 102(b) rejection to claims 1, 5-15, and 17-25, and request allowance of these claims.

CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 1, 5-15, and 17-25 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 1, 5-15, and 17-25 is respectfully requested.

No fees are required under 37 C.F.R. 1.16(b)(c). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 50-0471.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Respectfully submitted,

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CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this paper or papers, as described herein, are being deposited in the United States Postal Service, as first class mail, in an envelope address to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 18th day of October, 2005.

By
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